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A CPU benchmarking characterization of ARM based processors

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Big science projects are producing data at ever increases rates. Typical techniques involve storing the data to disk, after minor filtering, and then processing it in large computer farms. Data production has reached a point where on-line processing is required in order to filter the data down to manageable sizes. A potential solution involves using low-cost, low-power ARM processors in large arrays to provide massive parallelisation for data stream computing (DSC). The main advantage in using System on Chips (SoCs) is inherent in its design philosophy. SoCs are primarily used in mobile devices and hence consume less power while maintaining relatively good performance. A benchmarking characterisation of three different models of ARM processors will be presented.

Keywords: High data throughput, Computing, Big Data, ARM System on Chips, Benchmarking

Характеристика тестирования центрального процессора на базе процессоров ARM

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Большие научные проекты генерируют данные на всё более возрастающих скоростях. Типичные методы включают в себя хранение данных на диске, после незначительного фильтрования, а затем их обработку на больших компьютерных фермах. Производство данных достигло той точки, когда требуется обработка в режиме on-line, чтобы отфильтровать данные до управляемых размеров. Потенциальное решение включает в себя использование низко затратных процессоров ARM с маленькой мощностью в больших массивах для обеспечения массивного распараллеливания для вычислений потока данных (DSC). Главное преимущество в использовании систем на одном кристалле (SoCs) присуще самой философии этой разработки. Системы на микросхеме, прежде всего, используются в мобильных устройствах и, следовательно, потребляют меньше энергии при своей относительно хорошей производительности. Дано описание тестирования трех различных моделей процессоров ARM.

Ключевые слова: высокая вычислительная пропускная способность, большие данные, система на ARM чипе, эталонные тесты

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1. Introduction

The term ”Big Data” has caught on in the mainstream media and science worlds. While this word in now ubiquitous and almost exhausted in it’s use it still identifies an important issue in the science community. Processing data is getting more difficult due to the shear amount being produced. In the year 2022 the ATLAS detector will be upgraded and in doing so will produce in the order of Petabytes per second of raw data [ATLAS C 2012 Letter of Intent..., 2012]. There is no feasible way to process this much data in a reasonable amount of time. This is largely due to external Input/Output (I/O) bottlenecks present in current super computing systems. A team at the University of the Witwatersrand, Johannesburg is actively involved in the development of a computing system which is both cost-effective and able to provide high data throughputs in the order of Gigabits per second. There are four widely accepted computing paradigms. The first, and most commonly known, is the High Performance Computing paradigm (HPC) which is focused on the raw number of calculations performed per second. The second is the Many Task Computing (MTC) which focusses on the number of jobs that can be completed in a given amount of time. Real Time Computing (RTC) involves very strict restrictions on execution times (such as air-bag sensors or process controls). Finally, a fourth paradigm called Data Stream Computing (DSC) involves the processing of large amounts of data with no off-line storage. The processing unit that the team at the University of the Witwatersrand is designing falls under this DSC paradigm and provides the motivation for this paper. In order to design a processing unit that is capable of handling high throughputs the system must be very well balanced. A better understanding of the SoCs is needed in order to achieve this. Presented below is a CPU benchmarking characterisation of three ARM based SoCs.

2. Hardware

Three ARM system on chips will be characterised. The Cortex-A7, Cortex-A9 and Cortex-A15 are available on the Cubieboard2, Wandboard and Odroid-XU+E platforms [Cubieboard 2013 Fedora 19..., 2013; Freescale..., 2009; Hardkernel,...2013]. The specifications of each board can be found in Tab. 1.

Table 1: Specifications of the ARM platforms.

	Cortex-A7	**Cortex-A9**	**Cortex-A15**
Platform	Cubieboard A20	Wandboard Quad	ODROID-XU+E
SoC	Allwinner A20	Freescale i.MX6Q	Samsung 5410
Cores	2	4	4 (+ 4 Cortex-A7)
Max. CPU Clock (MHz)	1008	996	1600
L2 Cache (kB)	256	1024	2048
Floating Point Unit	VFPv4 + NEONv2	VFPv3 + NEON	VFPv4 + NEONv2
RAM (MB)	1024	2048	2048
RAM Type	432 MHz 32 bit DDR3	528 MHz 64 bit DDR3	800 MHz 64 bit DDR3
Ethernet (Mb/s)	100	400	100
PCI-Express (Gb/s)	-	5	-
2014 Retail (USD)	65	129	169

3. CoreMark

CoreMark was developed by The Embedded Microprocessor Benchmark Consortium (EEMBC) and has been proposed as the replacement for Drystone by ARM Holdings [Dunn and Marini, 2009]. The benchmark is specifically designed for Embedded Microprocessors which makes it an ideal benchmark to use. There are numerous pros to using CoreMark and they are summarised by Eric Schorn, VP marketing, Processor Division, ARM ”We believe that CoreMark represents a significant

improvement on the current Dhrystone benchmarks by measuring processor behaviour that could more realistically be expected in a real application. Combined with greater access to the results, this new benchmark should enable developers to obtain an unambiguous representation of processor performance enabling comparisons between competing processors to be made." [Dunn and Marini, 2009].

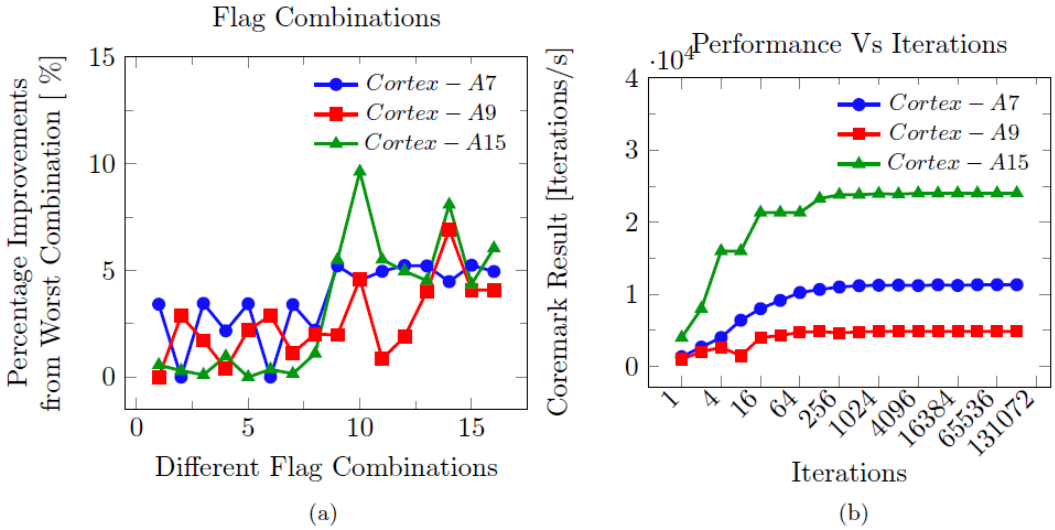

Fig. 1: a) Different flag combinations for compiling and b) Coremarks as a function of Iteration counts

CoreMark uses four common algorithms found in realistic applications such as matrix manipulation, linked list manipulation, state machine operations and cyclic redundancy checks. This provides an overall ''realistic" performance of the chips. Additionally, Coremark has strict online result submission guidlines. This provides a trustworthy and strong database of results with which to compare your own chips. The result is reported as the number of iterations of these four common algorithms per second. Figure 1a) shows the performance of different combinations of compiler flags. The best performing flag combinations can be seen in Tab. 2

Table 2: Best Performing Flag Combinations

Architecture	Flag Combination
Cortex-A7	-mfloat-abi=hard -ffastmath -O3 -mfpu=neon-vfpv4 -march=armv7-a -mtune=cortex-a7
Cortex-A9	-mfloat-abi=hard -ffastmath -O3 -mfpu=neon -march=armv7-a
Cortex-A15	-mfloat-abi=hard -ffastmath -O3 -mfpu=neon-vfpv4 -march=armv7-a

Figure 1b) shows the performance rise to a plateau for increasing iteration count. A particular criteria for result submission is to run the test for at least 10 seconds. This will be at approximately 2048 iterations and is well onto the plateau which illustrates why the database results are a fair comparison.

Figure 2 shows CoreMark results for various different systems. The first three bars represent the Cortex-A7, A9, and A15 results that we measured ourselves and the last four are from the CoreMark online database [EEMBC OnlineDatabase...]. The chosen systems are: a low powered Intel Atom 330, Intel Atom N2800, mid range Intel i7 2600 and a high end Intel i7 3930k. From Figure 2a) it can been seen that the high end Intel i7's are much more powerful per core. The Cortex-A9 is similar to the Atom 330 and like wise the Cortex-A15 is similar to the Atom N2800. Both sets of chips were manufactured around the same time. It must be noted that the Atom N2800 only has two cores while the Cortex-Al5 has four, which means that the overall performance of the Cortex-Al5 will still be better. Looking at the performance per watt in Fig 2b) the complete opposite is observed with the Cortex-A15 being over 3 times more efficient than the Intel i7 3930k. The power consumption measured for the Cortex chips included all peripherals while the Thermal Design Power is quoted for the Intel chips. This means the power consumption of the Intel chips would most likely increase when taking into account all peripherals.

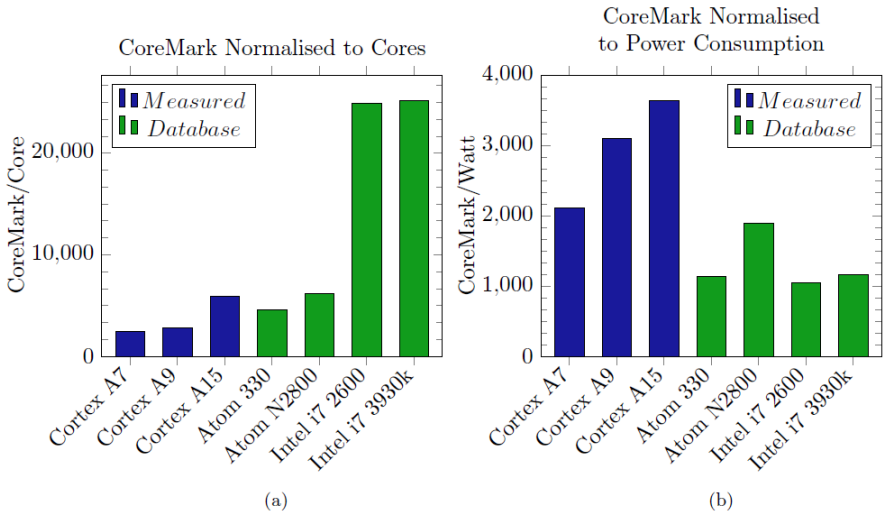

Fig. 2: a) CoreMark results for various systems normalised to the number of cores and b) CoreMark per Watt for various systems

4. High Performance Linpack

Coremark gives an overall performance of a system but to understand the computing capability one must use a benchmark like High Performance Linpack. This benchmark uses matrix manipulations to give the number of Floating Point Operations Per Second (FLOPS) that a system can achieve in double precision [Dongarra et all, 2003]. It was introduced by Jack Dongarra in l979 and first reported in the LINPACK Users Guide [Dongarra et all, 1979]. HPL is currently being used on the TOP500 Super-Computing List [TOP500, 2013] which makes the benchmark a necessity when characterising the ARM CPUs since its largely accepted and understood. HPL is scalable and specifically targeted at distributed memory clusters. An important measurement is the number of FLOPS measured per Watt of the system. This can be used to compare to the GREEN500 [GREEN500, 2013] which is a super-computing list based on efficiency rather than pure performance with results measured in GFLOPS/Watt.

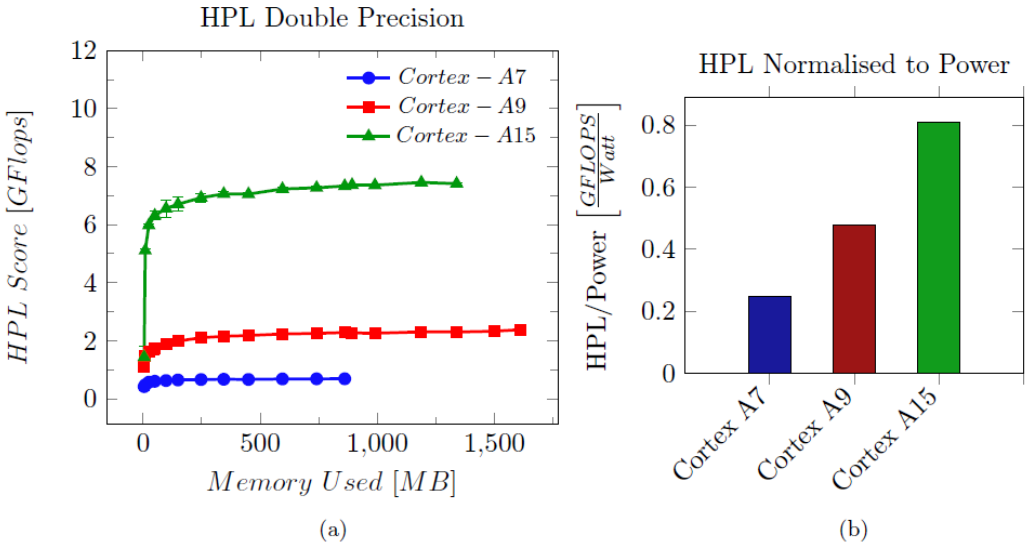

Fig. 3: Double precision High Performance Linpack results for Cortex-A7, Cortex-A9 and Cortex-A15

Figure 3a) shows the typical results reported by HPL for double precision floating point numbers. For clarity the array size (x-axis) is shown as the amount of memory used rather than the actual NxN matrix size. The Cortex-A15 performs the best with a GFLOP score over 3 times higher than the Cortex-A9. The Cortex-A7 is designed to be low performance with low power consumption so it's not surprising that it achieves approximately 0.8 GFLOPS. For very small array sizes (small sizes in RAM) there are large overheads when HPL is running. This is expected to be due to the calculation on given small arrays being shorter than the time taken to populate and fetch data from RAM.

Figure 3b) shows the double precision HPL Efficiency expressed as GFLOPS/Watt. The best performing result is taken. The Cortex-A15 is not 3 times the efficiency of the Cortex-A9. It is only a factor of 1.8. The Cortex-A15 attains a peak of 0.87 GFLOPS/Watt. This would be placed at 110th spot in the Green500 list [Green500-Top200, 2013]. Its interesting to see that the performance efficiency doubles from one architecture to the next. It is surprising to see that the Cortex-A7 has such low efficiency but this is attributed to all the external peripherals that increase the power consumption.

5. FFTW

The Fastest Fourier Transform in the West (FFTW) is a benchmark based on the discrete Fourier transform [Rajovic et all, 2013]. This type of transform is unique in that it has a finite number of elements and thus can be solved computationally. The transform allows a change of domain for a given set of data. The FFTW reports data in MFLOPS = (5Nlog10N)/t, where N is the size of the FFT and t is the time taken to compute the FFT. This is a theoretical performance but found to be quite accurate as it can be compared to results obtained for HPL. A second result reported is the throughput. Using the size of the FFT and the time taken to compute the MB/s throughput can be calculated. This is useful in the context of Data Stream Computing.

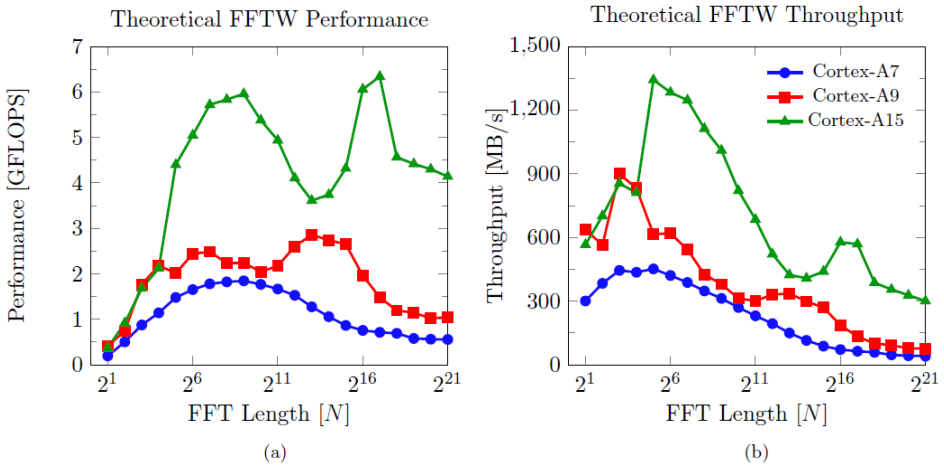

Fig. 4: FFTW benchmarks for the ARM Cortex-A7, A9 and A15 showing best-case multi-core and multi-process performance (a) and theoretical FFT throughput (b)

Figure 4a) shows the performance for various FFT sizes, N. It can be seen that the peak performances are similar to that of HPL in Fig. 3a). The shape is not smooth and this is due to the CPU specific components such as cache sizes, memory controllers and architectures. Figure 4b) shows the theoretical throughput that could be achieved if there were no bottle necks. Unfortunately the I/O performance is drastically limiting. Table 1 shows the connectivity of each SoC. The Cortex-A15 and Cortex-A7 both are limited to 1 Gb Ethernet while the Cortex- A9 has a PCIe lane at 5 Gb. For larger N values around 2^{16} we see the SoCs reaching the 1 Gb throughput range. The Cortex-A15 has a secondary peak at this point in the order of 5 Gb. This indicates that a Cortex-A15 could saturate a single PCIe lane for complex FFT problems.

6. Conclusion

The performance of the Atom is comparable to the Cortex A9 but looking at the power consumption it can be seen that the Atoms are less power efficient. The power consumption of the Atoms is based on their chip specifications alone so taking into account the need for a motherboard and all peripherals this is expected to increase. The Cortex-A7 does not have sufficient performance as seen in the HPL results in Fig 3a. There are newer ARM cores available such as the Cortex-A50 series [Holdings A Cortex-A50...] and new Atoms such as the Z34XX Series [Intel..., 2014] which will usher in the 64 bit architectures. The new Atoms are SoCs and the power consumption will be better than the Atoms shown in this paper. These new ARM architectures will have double precision NEON extensions which will drastically increase their performance as current NEON extensions are only single precision. Intel have opened their fabrication plants to the new Cortex-A53 on their 12 nm trigate technology [Martenson, Altera, 2013] so the expected performance of these ARM CPUs and possibly the newer Atoms will increase significantly and could offer a cheaper alternative for parallel computing. The same can be said for the new generation of Atoms.

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